Abstract -- Low power has emerged as a principal theme in today's electronic industry. Reduction of power consumption makes a device more reliable and efficient. As the demand of portable consumer electronics increases, and the size of the chip decreases, challenges towards the power dissipated are induced. Complementary Metal Oxide Semiconductor (CMOS) logic styles are best known for dissipating less energy or low power. The Proposed topology aims to design comparator logic circuits with different logic styles such as conventional CMOS, dynamic CMOS and domino CMOS. Initially, a single bit comparator will be designed and its functionality will be verified with all the three kinds of styles mentioned above. Using this design, by connecting them in a cascaded fashion, higher bit comparator circuits (4-bit and 8-bit) shall be obtained and a comparison will be drawn between the existing technology and the proposed design.

Keywords: CMOS logic, Comparators, Dynamic logic, dynamic CMOS, Low power

I. INTRODUCTION

A comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. If the +ve VP, the input of the comparator is at a greater potential than the -ve VN, input, the output of the comparator is a logic 1, where as if the +ve input is at a potential less than the –ve input, the output of the comparator is at logic 0.

If VP < VN then VO = VSS= logic 0.
If VP > VN then VO = VDD= logic 1.

II. LITERATURE REVIEW

According to Moore’s Law, since the number of transistors integrated in a chip doubles once in every 18 months, thus, the role of circuit designers become very crucial. Decades ago, Speed and area were the important constraints and not power because the number of transistors involved in a design were quite less around hundreds or thousands, but in the present scenario, as the complexity of the chips increase, millions of transistors are integrated in order to achieve the task with more functionalities and features. Hence, the power Dissipation of the overall chip or product is an extremely large value and has to be reduced significantly using suitable design techniques. This can be achieved by a number of ways such as reducing the number of transistors i.e. modifying the design which occupies a lesser number of transistors for the same functionality.

The main objective of this paper is to implement the higher bit comparator circuits with fewer transistors so that the total power dissipation will be reduced. We have implemented comparator circuits using conventional CMOS (Complementary Metal Oxide Semiconductor) and dynamic CMOS logic styles. Conventional CMOS technology implementation offers low power because of the nmos and pmos transistors behavior. While the pull

Figure 1. Comparator Operations.

Figure 1.(a) Karnaugh map for a one – bit comparator.
Figure (b). Block diagram of a One – bit comparator.

up network is on, the pull down network is off and vice versa. So, the static power dissipation is ideally zero.
This is the biggest advantage of the CMOS VLSI technology compared to other systems such as GaAs.

Also, as a part of this paper, we design the comparator circuits using efficient XOR gates especially implementing XOR function with a fewer number of transistors. This is one kind of method to implement low power, low energy systems. Since the overall power is directly proportional to the layout area occupied by the design, this technique will be an efficient one. Hence designing with lesser transistors in turn will reduce the layout size of the design.

We shall focus more on 4-bit comparator circuit design by connecting 1-bit comparators in a cascaded fashion. Also, an 8-bit comparator will be tried to implement using corresponding 4-bit comparators.

II. SINGLE BIT COMPARATOR

The 1-bit comparator is designed with the desired output GT (greater than), LT (Lesser than) and EQ (equal). Considering the inputs to be A and B, the desired outputs are to be GT: A>B, LT: A<B and EQ: A=B. Using k-map we can solve for the above as GT=AB', LT=A'B and EQ = AB+A'B'. The k-map and circuit diagram of a single-bit comparator is as shown.

III. EFFICIENT XOR/XNOR GATES

The XOR logic expression AB'+A'B can be implemented using the conventional CMOS logic style with 14 transistors. This is too high for a simple design and dissipates more power since the number of transistors is more. We shall implement some alternative designs for XOR gate so that a few transistors can be used, thereby; low power or energy dissipation is achieved. Pass transistor logic helps to design a gate with less number of transistors.

Pass Gate logic (Model 1)

IV. 4-BIT AND 8-BIT COMPARATOR SCHEMATIC DESIGNS

A 4-bit comparator can be easily designed by cascading the four 1-bit comparators and using one 4-input OR gate and NOR gate. The schematic diagram of a 4-bit comparator is shown. The inputs are to be given according to the need and the output is obtained at the resulting LED. Similarly, we can cascade eight 1-bit comparators to obtain an 8-bit comparator. Also, this can be achieved using cascade connection of 4-bit comparators.

V. SIMULATIONS

An OrCAD PSpice tool is used as the simulator application for the analysis and performance verification of the various CMOS comparator configurations. The input signals and relevant clock signals are supplied by the tool automatically and the result is verified. The OrCAD tools are known to be extremely useful for the study of analog and mixed signal digital circuits.
a) 8-bit Comparator Circuit Diagram in simulating software

b) Schematic of conventional CMOS comparator using 20 transistors and Power Plot
c) Existing CMOS comparator technology using 12 Transistors

d) Schematic of the proposed Comparator Design and Power Plot
VI. SIMULATION RESULTS
Table 1 depicts power consumption of the three models simulated with the respective number of transistors used.

TABLE 1 -- COMPARISON TABLE OF POWER DISSIPATION FOR 8-BIT COMPARATOR MODELS

<table>
<thead>
<tr>
<th>S.N.</th>
<th>Comparator Model</th>
<th>Number of Transistors Employed</th>
<th>Dynamic Power Dissipated</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>Conventional CMOS based Comparator</td>
<td>182</td>
<td>8 mW</td>
</tr>
<tr>
<td>02</td>
<td>Existing Model</td>
<td>118</td>
<td>1.16 nW</td>
</tr>
<tr>
<td>03</td>
<td>Proposed Design</td>
<td>102</td>
<td>125.25 pW</td>
</tr>
</tbody>
</table>

VII. CONCLUSION
The proposed design with a fewer number of transistors using pass-transistor logic offers less power dissipation in contrast to the existing conventional techniques. The decrease in power dissipation is credited to the reduced number of transistors and the increase in power dissipation in dynamic logic circuits is due to the increased number of transistors and the clocking circuitry.

Most of the times, speed, area and power are the three important VLSI optimization goals for any kind of design. There may be a trade-off with speed and power, but still low power or energy, designs are preferred over high speed logic circuit designs.

VIII. SCOPE FOR FUTURE WORK
In today’s world, where demand for portable battery operated devices is increasing, a major thrust is given towards low power methodologies for high speed applications. This reduction in power can be achieved by moving towards smaller feature size processes. However, as we move towards smaller feature size processes, the process variations and other non-idealities will greatly affect the overall performance of the device. One such application where low power dissipation, low noise, high speed, less Offset voltage are required is Analog to Digital converters for mobile and portable devices.

IX. ACKNOWLEDGEMENT
Authors express profound gratitude to Mr. P.K. Sinha, Professor, Maharaja Agrasen Institute of Technology, New Delhi, India for his invaluable guidance, support and useful suggestions at every stage of this work.

X. REFERENCES


